PROCESS FOR ETCHING POLYSILICON GATES WITH GOOD MASK SELECTIVITY, CRITICAL DIMENSION CONTROL, AND CLEANLINESS

The present invention provides a process of etching polysilicon gates using a silicon dioxide hard mask. The process includes exposing a substrate with a polysilicon layer formed thereon to a plasma of a process gas, which includes a base gas and an additive gas. The base gas includes HBr, Cl_2, O_2, and the additive gas is NF_3 and/or N_2. By changing a volumetric flow ratio of the additive gas to the base gas, the etch rate selectivity of polysilicon to silicon dioxide may be increased, which allows for a thinner hard mask, better protection of the gate oxide layer, and better endpoint definition and control. Additionally, when the polysilicon layer includes both N-doped and P-doped regions, the additive gas includes both NF_3 and N_2, and by changing a volumetric flow ratio of NF_3 to N_2, the etching process may be tailored to provide optimal results in N/P loading and microloading.